AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a pattern forming region and a pattern non-forming region;

a wiring pattern formed on said pattern forming region;

a plurality of dummy patterns formed on said pattern non-forming region, said plurality of dummy ~~patters~~ patterns being formed within a plurality of ~~standard~~ dummy areas each having a same shape; and

an insulating film formed on said wiring pattern and said plurality of dummy patterns;

wherein each of said plurality dummy patterns is spaced apart with a width filled by plus sizing of said insulating film formed on said plurality of dummy patterns.

2-4. (Cancelled)

5. (Currently Amended) A semiconductor device according to claim 1, wherein the ~~standard~~ dummy areas each have a square shape.

6. (Currently Amended) A semiconductor device according to claim 1, wherein the ~~standard~~ dummy areas are arranged in lattice form.

7. (Previously Presented) A semiconductor device according to claim 1, wherein the width is approximately less than 72 μm.

8. (Previously Presented) A semiconductor device according to claim 1, wherein said plurality of dummy patterns are line patterns.

9. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a pattern area and a non-pattern area;

a conductive pattern formed on said pattern area of said semiconductor substrate; and

a plurality of dummy patterns formed on said non-pattern area of said semiconductor substrate, each of said plurality of dummy patterns having a ~~standard~~ same rectangular outline as each other and being arranged in a matrix with predetermined spacing;

wherein each of said plurality of dummy patterns has an opening so that a pattern ratio of said semiconductor device is reduced.

10. (Previously Presented) A semiconductor device according to claim 9, wherein each of said plurality of dummy patterns has a square outline.

11. (Previously Presented) A semiconductor device according to claim 9, wherein the opening has a square outline.

12. (Previously Presented) A semiconductor device according to claim 9, wherein the opening has a shape of a letter.

13. (Previously Presented) A semiconductor device according to claim 9, wherein the opening has a shape of a plurality of letters.

14. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a pattern area and a non-pattern area;

a conductor pattern formed on said pattern area of said semiconductor substrate;

a plurality of dummy patterns formed on said non-pattern area of said semiconductor substrate;

wherein each of said plurality of dummy patterns are formed in a plurality of ~~standard~~ dummy areas each having a same shape and being arranged in a matrix with predetermined spacing; and

wherein each of said plurality of dummy patterns has a space portion within each of the ~~standard~~ dummy areas so that a pattern ratio of said semiconductor device is reduced.

15. (Previously Presented) A semiconductor device according to claim 14, wherein each of said plurality of dummy patterns has a rectangular outline and an opening at the space portion.

16. (Previously Presented) A semiconductor device according to claim 15, wherein the opening has a square outline.

17. (Previously Presented) A semiconductor device according to claim 15, wherein the opening has a shape of a letter.

18. (Previously Presented) A semiconductor device according to claim 15, wherein the opening has a shape of a plurality of letters.

19. (Currently Amended) A semiconductor device according to claim 14, wherein said plurality of dummy patterns are line patterns, and each of the ~~standard~~ dummy areas has line patterns spaced apart from each other.

20. (Previously Presented) A semiconductor device according to claim 19, wherein the line patterns are arranged with a space therebetween being approximately less than 72 μm.